ABSTRACT OF THE DISCLOSURE

An internal call/return stack (CRS) correction apparatus in a pipelined microprocessor is disclosed. Each time the microprocessor updates the CRS in response to a call or return instruction (call/ret), the microprocessor also stores correction information into a first correction stack. The microprocessor includes two distinct stages that detect invalidating events, such as a branch misprediction or exception. Once a call/ret passes the first detecting stage, the correction information associated with that call/ret is moved from the first correction stack to a second correction stack. If an invalidating event is detected at the upper detecting stage, then only the correction information in the first stack is used to correct the CRS. However, if an invalidating event is detected at the lower detecting stage, then the correction information in both the first and second stack is used to correct the CRS.